REMARKS

This application has been reviewed in light of the Office Action dated March 22, 2006. Claims 1-11 and 18-34 are pending in this application. Claims 1, 18, 22, 26-28, and 32-34, all of which are independent claims, have been amended to define still more clearly what Applicant regards as his invention. Favorable reconsideration is requested.

Claims 1-11, 19-21, 23-26, and 32 were rejected under 35 U.S.C. § 103(a) as being obvious from U.S. Patent No. 5,838,678 (Davis et al.) in view of U.S. Patent 6,262,990 (Ejiri) and further in view of U.S. Patent No. 6,058,109 (Lechleider); and Claims 18, 22, 27-31, 33, and 34, as being obvious from Davis in view of Ejiri.

Applicant submits that independent Claims 1, 18, 22, 26-28, and 32-34, together with the remaining claims dependent therefrom, are patentable over the cited references for at least the following reasons.

It is believed that the general nature of the invention has been adequately discussed in previous papers, and that discussion will not be repeated.

Claim 1 is directed to an information processing apparatus that includes input means for inputting variable length packet data including packet length information indicative of a packet length and encoded information data, and judgment means for judging the packet length of the variable length packet data. Packet generating means generates the variable length packet data into fixed length packet data in accordance with an output of the judgment means, and transmits the fixed length packet data. The packet generating means includes memory means for generating fixed length data and initializing means for initializing beforehand the memory means by writing stuffing data in the

memory means. The packet generating means generates the fixed length data by overwriting the variable length packet data into the initialized memory means in accordance with the packet length judged by the judgment means and reads out the data from the memory means. In addition, the packet generating means generates the fixed length packet data in which the stuffing data is written, in case that the variable length packet data to be written into the memory means is shorter than a predetermined length.

Among other notable features of Claim 1 are that an information processing apparatus is arranged to initialize beforehand memory means by writing stuffing data in the memory means (see, e.g., step S203 of the present application), and generate fixed length data by overwriting variable length packet data into the initialized memory means in accordance with a judged packet length.[1]

Davis et al., as understood by Applicant, relates to pre-processing streams of encoded data to facilitate decoding streams back to back. In Fig. 9, cited in the Office Action, private data packets are inserted into buffer memory 932 before, after, or within pre-processed transport stream file(s) 940 (see, e.g., col. 10, lines 30-38).

Ejiri, as understood by Applicant, relates to a transmission system which multiplexes a plurality of data of different rates into a fixed length packet to be transmitted. More specifically, Ejiri discusses periodically generating a release timing signal which is in inverse proportion to the rate, to transmit data stored in a buffer memory as the fixed length packet data.

---

[1]It is of course to be understood that the references to various portions of the present application are by way of illustration and example only, and that the claims are not limited by the details shown in the portions referred to.

At page 3 of the Office Action, the Examiner states: "Davis nor Eijiri teach stuffing data into the memory before generating the fixed length packet." In this way, the Examiner concedes that Davis and Eijiri fail to teach writing stuffing data into a memory to initialize the memory. The Examiner then cites Lechleider as allegedly teaching "stuffing data into a buffer to compensate for lack of enough data" (see page 3 of the Office Action).

Lechleider, as understood by Applicant, relates to a combined uniform rate and burst rate transmission system. Lechleider discusses switching over a burst data stream and a uniform rate data stream to transmit them on a single transmission line (see, e.g., Fig. 2 and the abstract). According to Lechleider, since an input rate and an output rate of a transmission buffer 250 (see Fig. 2) are different from each other (see column 6, line 59, to column 7, line 2), null packets are supplied into the buffer. For example (see Fig. 9), when electric power is turned on, three null packets are written into the buffer, and then during the time period 0-1, two of the written three null packets are transmitted and thereafter a packet 1 and an additional null packet are written into the buffer. During the next time period, the remaining one of the initially-written three null packets and the written packet 1 are transmitted.

However, when the electric power is turned on, the null packets are not written into the whole area of the buffer 250 and thus the buffer is not initialized beforehand to generate transmission data. That is, the buffer operates as a FIFO memory, and the null packets written into the buffer are all output therefrom (see, e.g., Fig.9). Lechleider therefore fails to teach or suggest initializing beforehand the buffer by writing the null packets into the buffer and then overwriting the packets into the initialized buffer to generate transmission data.

Nothing in Davis et al., Ejiri, or Lechleider, whether considered separately or in any permissible combination (if any), would teach or suggest initializing beforehand memory means by writing stuffing data in the memory means, and generating fixed length data by overwriting variable length packet data into the initialized memory means in accordance with a judged packet length, as recited in Claim 1.

Accordingly, Applicant submits that Claim 1 is patentable over Davis et al., Ejiri, and Lechleider, whether considered separately or in any permissible combination (if any).

Independent Claims 26 and 32 recite features similar in many relevant respects to those discussed above with respect to Claim 1 and therefore are also believed to be patentable over Davis et al., Ejiri, and Lechleider for at least the reasons discussed above.

Claim 18 is directed to an information processing apparatus that includes first generating means for generating variable length packet data including encoded information data, second generating means for generating and transmitting first fixed length packet data from the generated variable length packet data, and generating means for generating clock reference information for use in a time reference during decoding of the encoded information data. The second generating means generates second fixed length packet data including the clock reference information and transmits the second fixed length packet data within a predetermined time interval, and compulsorily transmits the second fixed length packet data regardless of the predetermined time interval if valid first fixed length packet data for transmission is not present.

Among other notable features of Claim 18 are that an information processing apparatus is arranged to generate clock reference information for use in a time reference during decoding of encoded information, generate second fixed length packet data including the clock reference information to transmit the second fixed length packet data within a predetermined time interval, and compulsorily transmit the second fixed length packet data regardless of the predetermined time interval if valid fixed length packet data for transmission is not present.

At paragraph 48 (page 12) of the Office Action, the Examiner states:

> Applicant also argues that nothing in Ejiri would teach or suggest determining a transmission timing dependent on whether data is present in the buffer or not. This limitation in the argument by applicant is not in the claims.

Claim 18 as amended recites that second fixed length packet data is compulsorily transmitted regardless of the predetermined time interval if valid fixed length packet data for transmission is not present. As such, Applicant hereby reiterates the Remarks set forth in the Preliminary Amendment filed on March 9, 2006.

Nothing in Davis et al. or Ejiri, whether considered separately or in any permissible combination (if any), would teach or suggest (1) generating clock reference information for use in a time reference during decoding of encoded information, (2) generating second fixed length packet data including the clock reference information to transmit the second fixed length packet data within a predetermined time interval, and (3) compulsorily transmitting the second fixed length packet data regardless of the predetermined time interval if valid fixed length packet data for transmission is not present, as recited in Claim 18.

Accordingly, Applicant submits that Claim 18 is patentable over Davis et al. and Ejiri, whether considered separately or in any permissible combination (if any).

Independent Claims 22, 27, 28, 33, and 34 recite features similar in many relevant respects to those discussed above with respect to Claim 18 and therefore are also believed to be patentable over Davis et al. and Ejiri for at least the reasons discussed above.

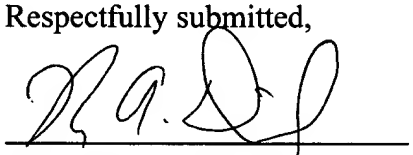
The other rejected claims in this application depend from one or another of the independent claims discussed above, and, therefore, are submitted to be patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, individual reconsideration of the patentability of each claim on its own merits is respectfully requested.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,



Raymond A. DiPerna
Attorney for Applicant
Registration No. 44,063

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200

NY_MAIN 577064v1